

Amphenol

COMMUNICATIONS SOLUTIONS

PCIe 6 Performance

Date: 2022.10.02

Rev.09



Commercial IO

-PCIe Roadmap

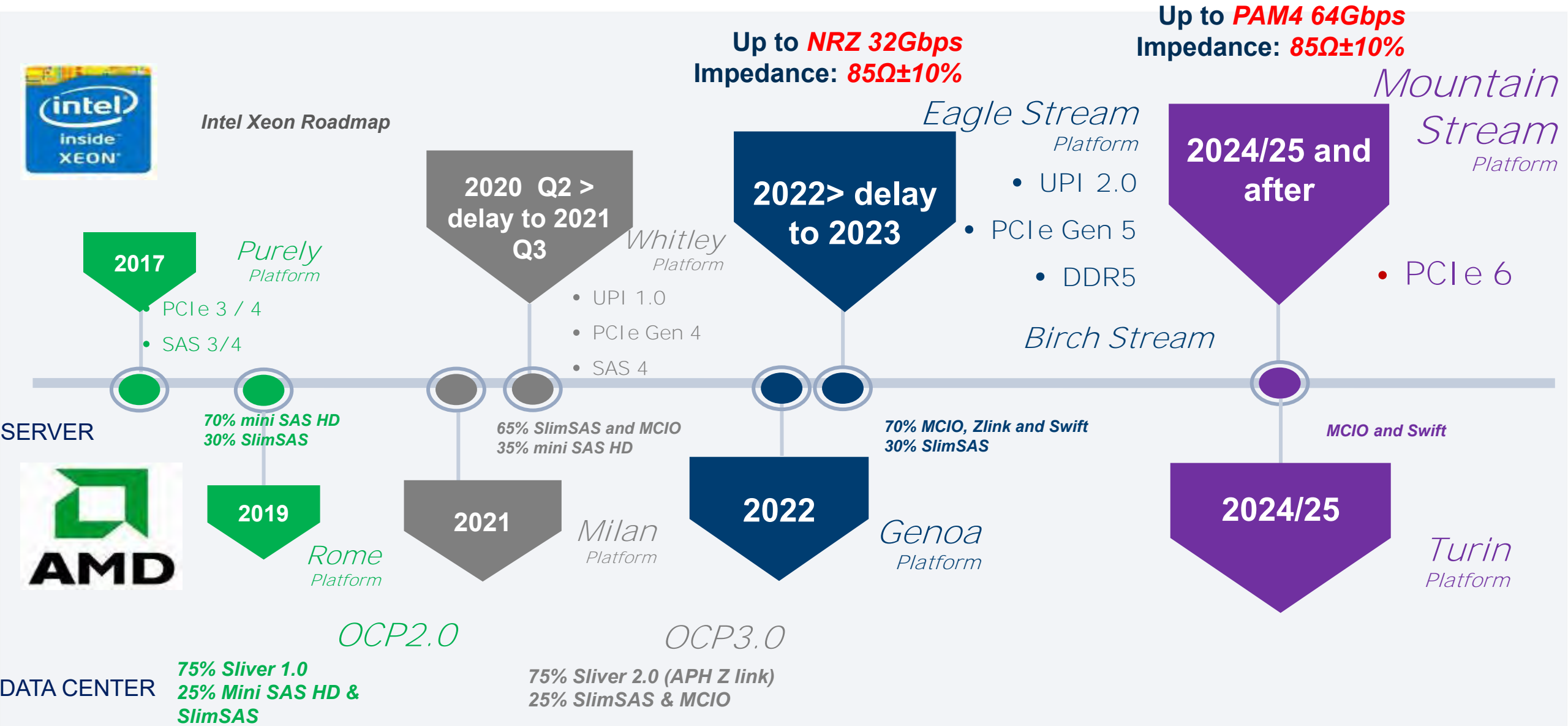
-Application

-Product introduction

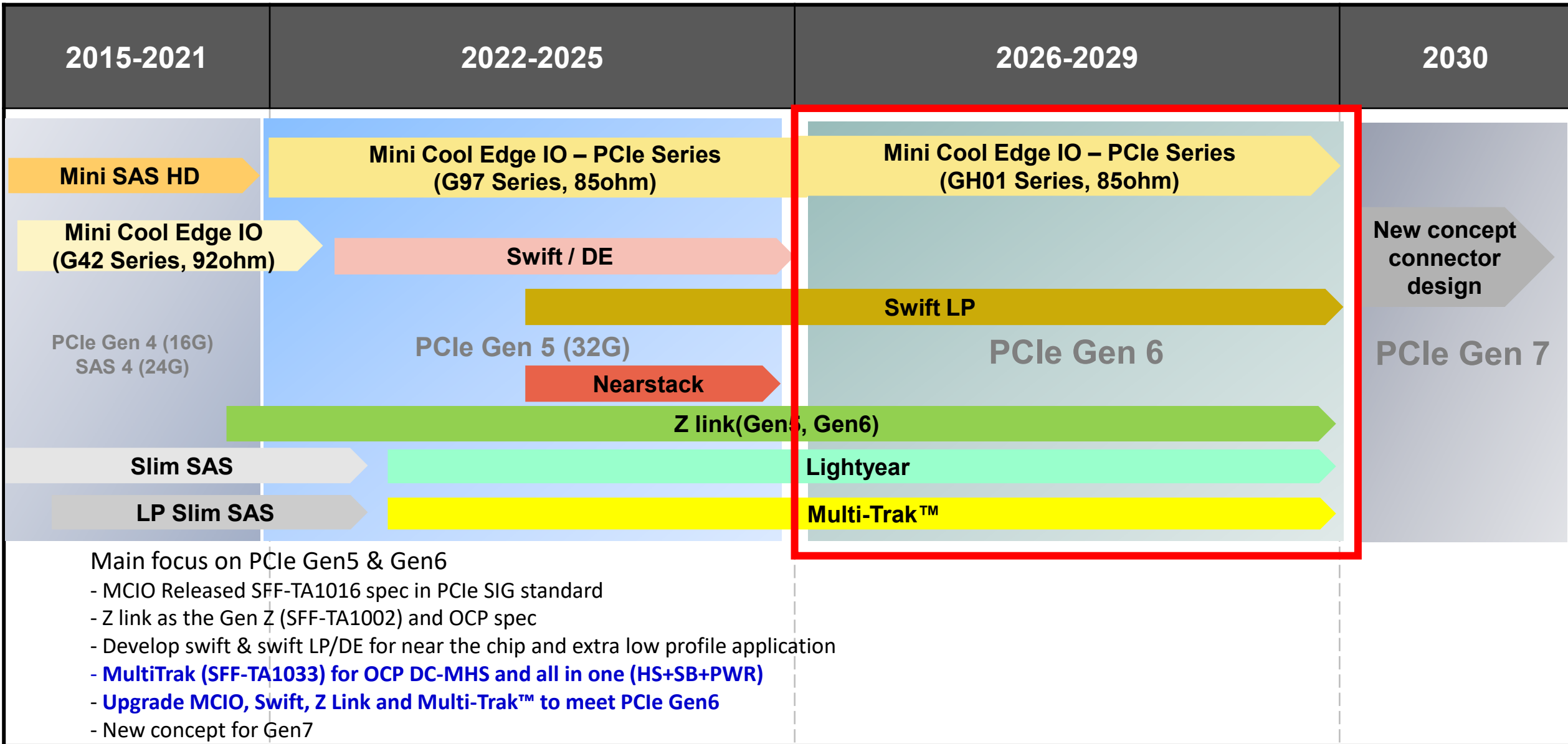
- ✓ MCIO
- ✓ Multi-Trak™
- ✓ Swift

-Why Amphenol?

Server CPU Roadmap



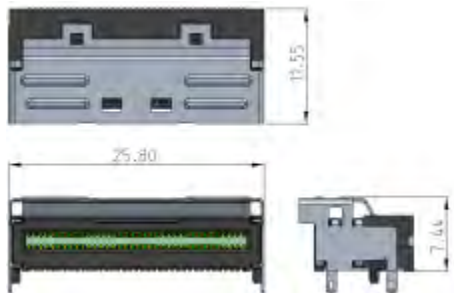
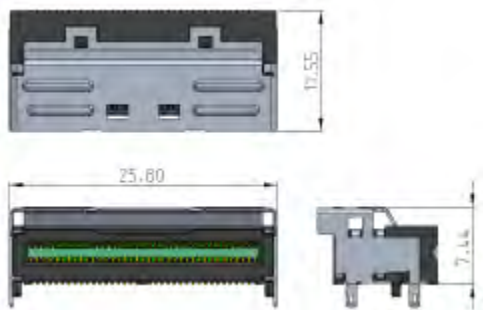
PCIe MP Trend– CMIO Gen6 Roadmap



industry

Standard

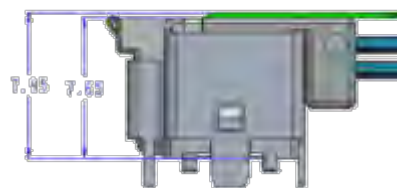
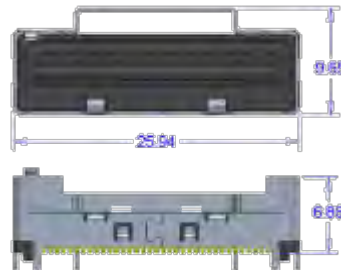
MCIO



ultra

Low Profile

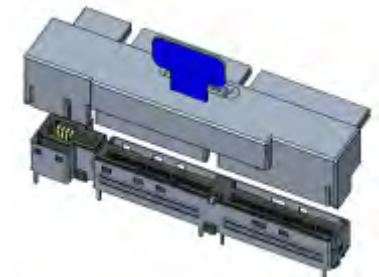
Swift LP



combo

All in one

Multi-Trak™



Mini Cool Edge IO

SFF-TA-1016, PCI SIG Gen5/Gen6, OCP DC-MHS

Mini Cool Edge IO for PCIe Gen6 (SFF-TA-1016)

Amphenol CS introduces to the market **SFF-TA-1016** standard interconnect solution – **Mini Cool Edge IO**, which is 0.60 mm pitch, slim form factor design yet capable of transmitting high-speed signal up to **64G** over the distance overwhelming the conventional routings.

The Mini Cool Edge IO provides not only a SI performance ready signal transmission media but also a new way of system design thinking that will lead your electronic system to a completely **cost effective, highly modularized & scalable**, and extremely **easy repairing** masterpiece.

Features

- Pitch **0.60 mm**, both V/T & R/A form factors
- Up to **PAM4 64Gbps**, over **1 m** transmission distance
- **Dual-use**, supporting both **cable and card** connection with one identical connector
- Optional **85Ω or 100Ω** impedance and variety of pin no. options – covering most common uses applications in data centers such as PCIe/NVMe/SAS/SFP(+)/SFP 28/...

Benefits

- Providing enhanced **flexibility** in system design to meet highly modularized, highly scalable, and easy repairing requirement simultaneously
- Real **economic** choice for not only save system material cost but also show high succession of system electrical design that saves both engineering and certification expenses



32Gbps
NRZ

Upgrade to PCIe GEN6

64Gbps
PAM4

Internal
Connection

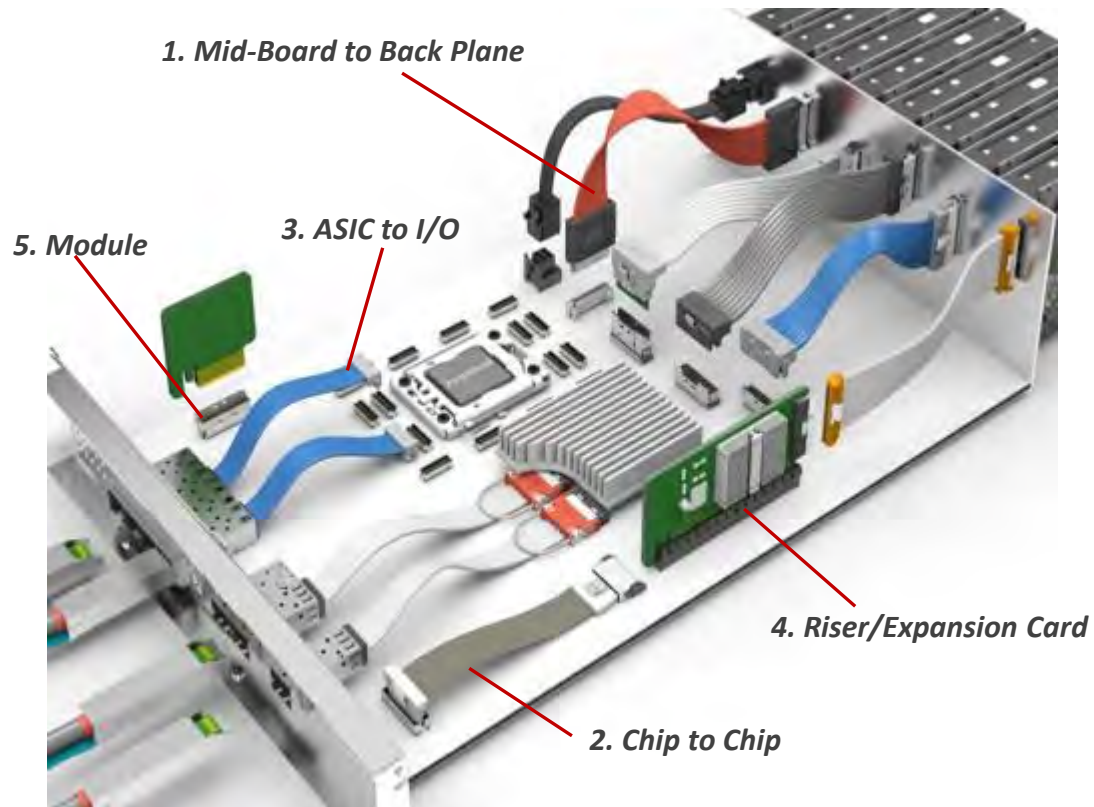
Blind Mate
(Floating) Connection

Data Center Applications Supported:

- ✓ **PCI-Express**
- ✓ **NVMe**

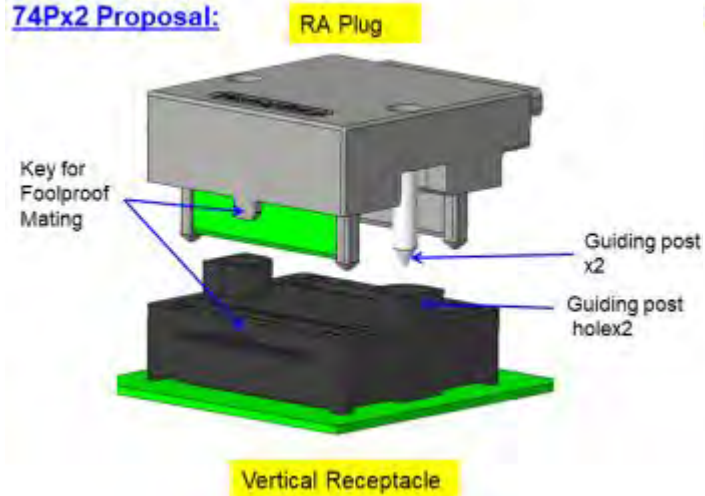
Multiple Form Factor
Wide Variety Solution Supported

Internal_ MCIO can support both card and plug mating.

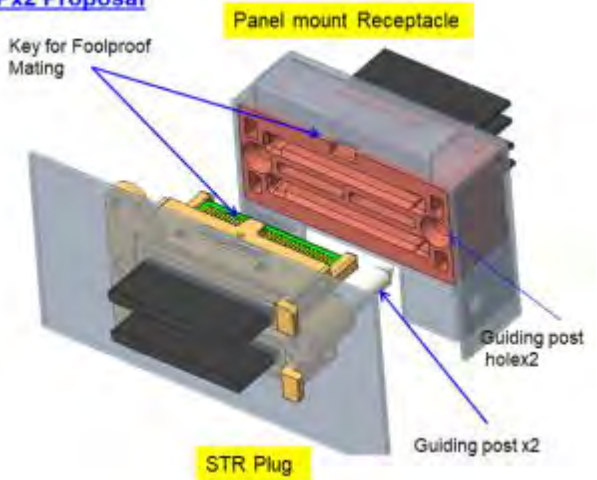


Blind Mating (Surelink)

Wire to Board
74Px2 Proposal:



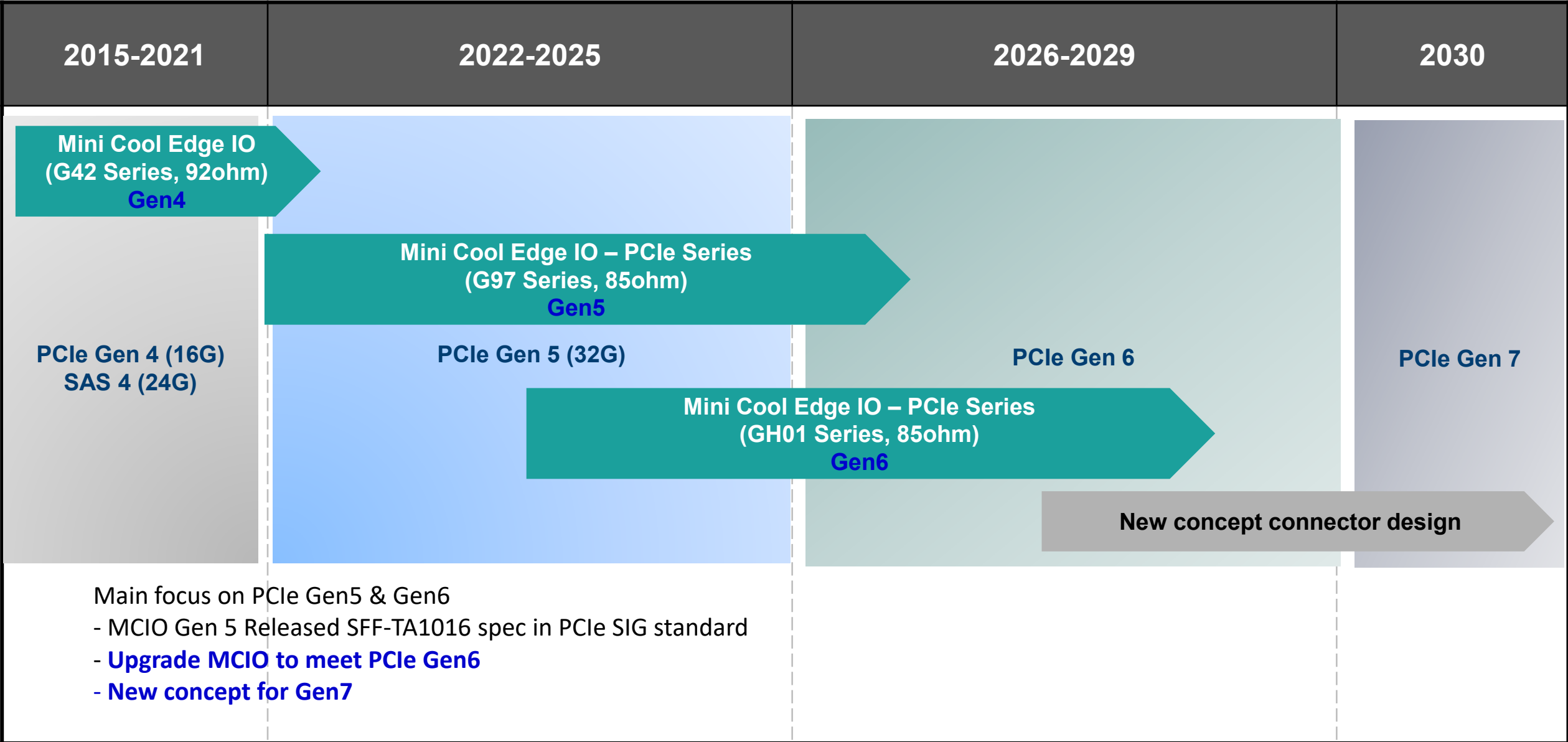
Wire to Wire
74Px2 Proposal



Comments:

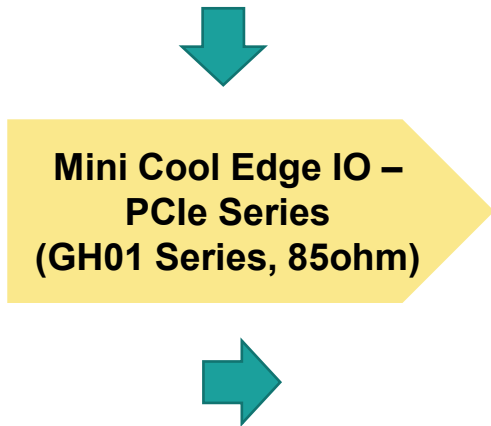
1. Plug and Receptacle need to be customized.
2. Using guide posts and chamfers of Receptacle to guide plug into receptacle.

PCIe Develop Roadmap Trend–MCIO



Roadmap – MCIO Gen6

- We have been tooled up Gen6 VT 8X and estimate have actual SI test result around in end of Q4.



Year		2022		2023				Remark
Form Factor	Pin	Q3	Q4	Q1	Q2	Q3	Q4	
V/T	38				4X			
	74	8X						
	124		16X					
	148							Tool up per requested
R/A	38				4X			
	74	8X						
	124						16X	
	148							Tool up per requested

Product Details – MCIO

PCIe Gen 6 (GH01* series)

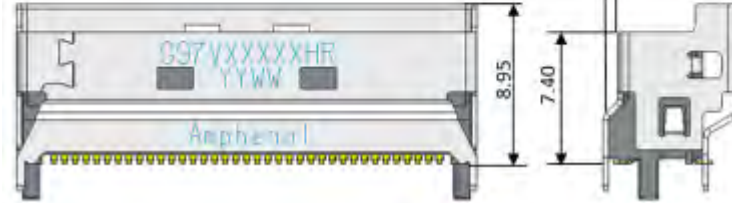
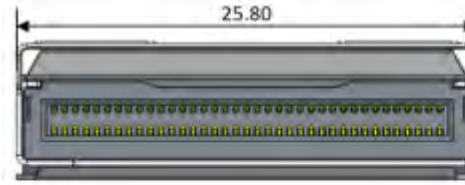
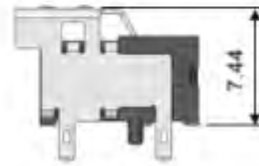
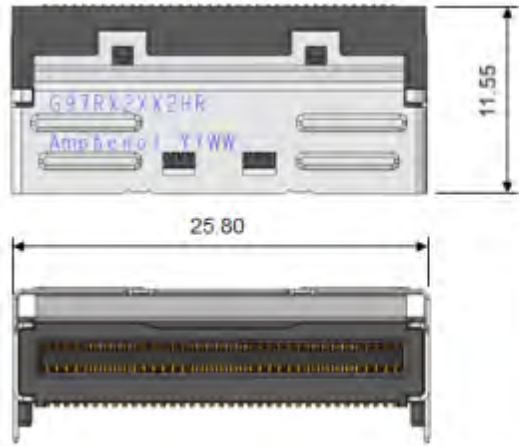
Spec	Form Factor	Pin	Recommended Channel: with Sideband	Pic	Width (mm)	Mating Height (mm)	Footprint
<ul style="list-style-type: none"> • PAM4 64G, 85Ω • Supports both Card (T 1.57 mm) & Cable connection) • Pitch 0.60 mm • Voltage Rating: 30V_{DC} • Operating Temperature: -25°C ~ 105°C • Storage Temperature: -55°C ~ 105°C • Ambient Humidity: 80% R.H. Maximum 	V/T	38	4x + Sideband		15.00	Right Angle Exit: 11.95~14.95 mm 	<p>RECOMMENDED PCB LAYOUT (GENERAL TOLERANCES :±0.05)</p>
		74	8x + Sideband		25.80		
		124	16x + Sideband		42.00		
	R/A	38	4x + Sideband		15.00	Straight Exit: 18.50 mm 	<p>RECOMMENDED PCB LAYOUT (GENERAL TOLERANCES :±0.05)</p>
		74	8x + Sideband		25.80		
		124	16x + Sideband		42.00		

Benefit _ Keep the same interface and footprint

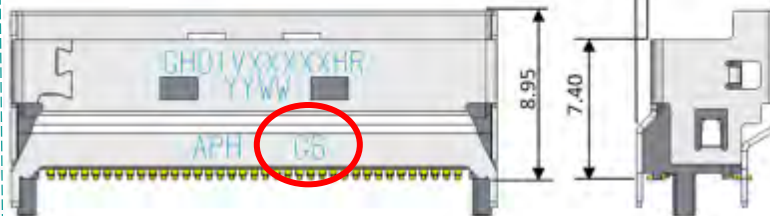
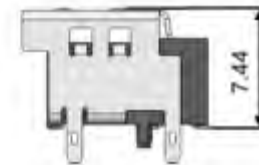
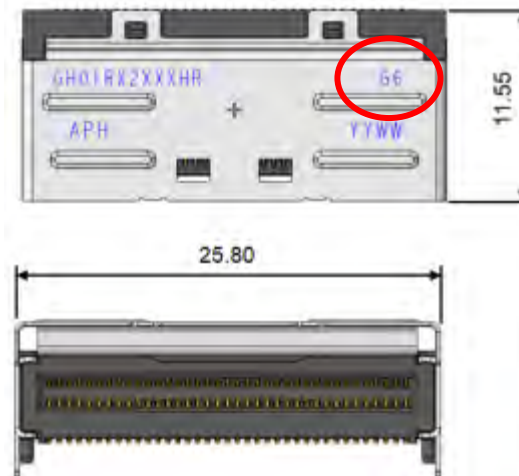
Right Angle

Vertical

PCIe
Gen 5

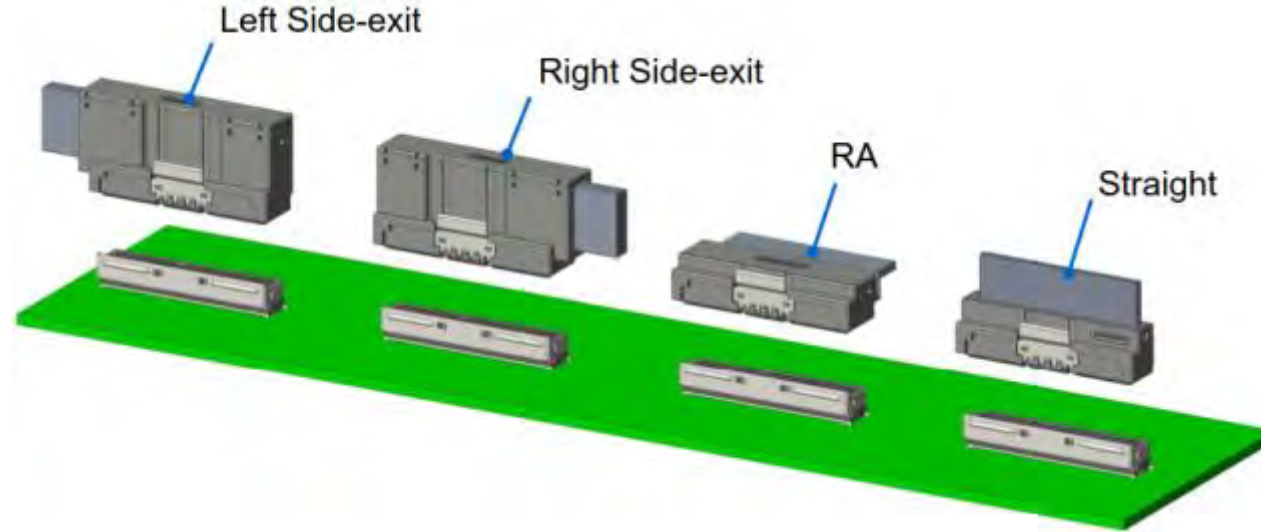


PCIe
Gen 6



- ✓ New design inner structure for PCIe Gen6.
- ✓ Keep same 0.6pitch, interface, outline dimension and footprint dimension.
- ✓ Upgrade SI to Gen 6 with pitch and interface limitation.
- ✓ Add “G6” mark for Gen6 version to identify Gen5 vs Gen6.

Multiple cable types to support wide variety of mechanical requirement.



Gen 4,5 version

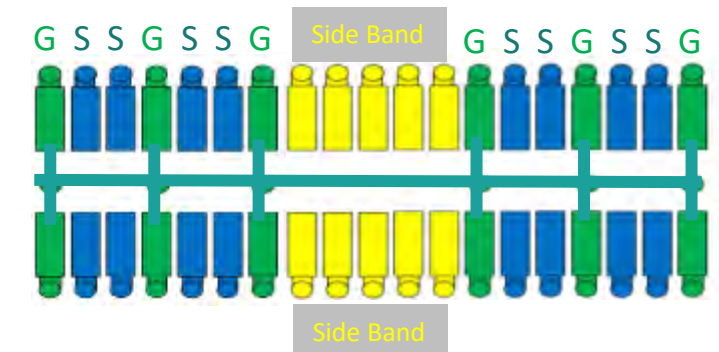
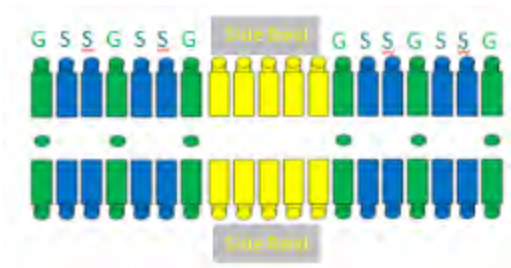
For 92ohm and 85ohm MCIO, We have full high-speed to different side band choices – extreme flexible on **customization pin define**.

Flexible on PIN define series(PN):

- MCIO 92ohm(Gen4 version)
- MCIO 85ohm(Gen5 version)

Gen 6 version

Gen6's GND Pin are connected together for better Crosstalk, so pin define is fixed.



Ex. 38PIN

- Option 1: 4 pair HS channel + side band
- Option 2: 6 pair HS channel
- Option 3.....

Benefit_ Co-developed with the association PCIe Committee Selection & better SI

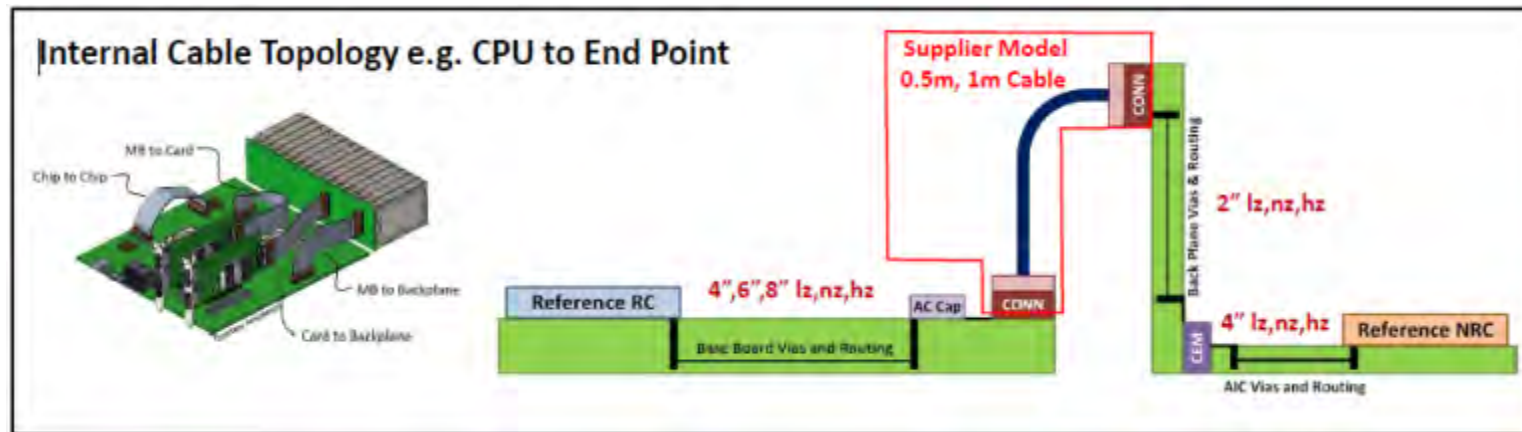
**Amphenol Feedback to EWG Ver 0.5
MCIO Cable Assembly Gen 5/6 SI Limit**

Amphenol
Jan 19, 2021

Copyright © 2020 PCI-SIG. All Rights Reserved.

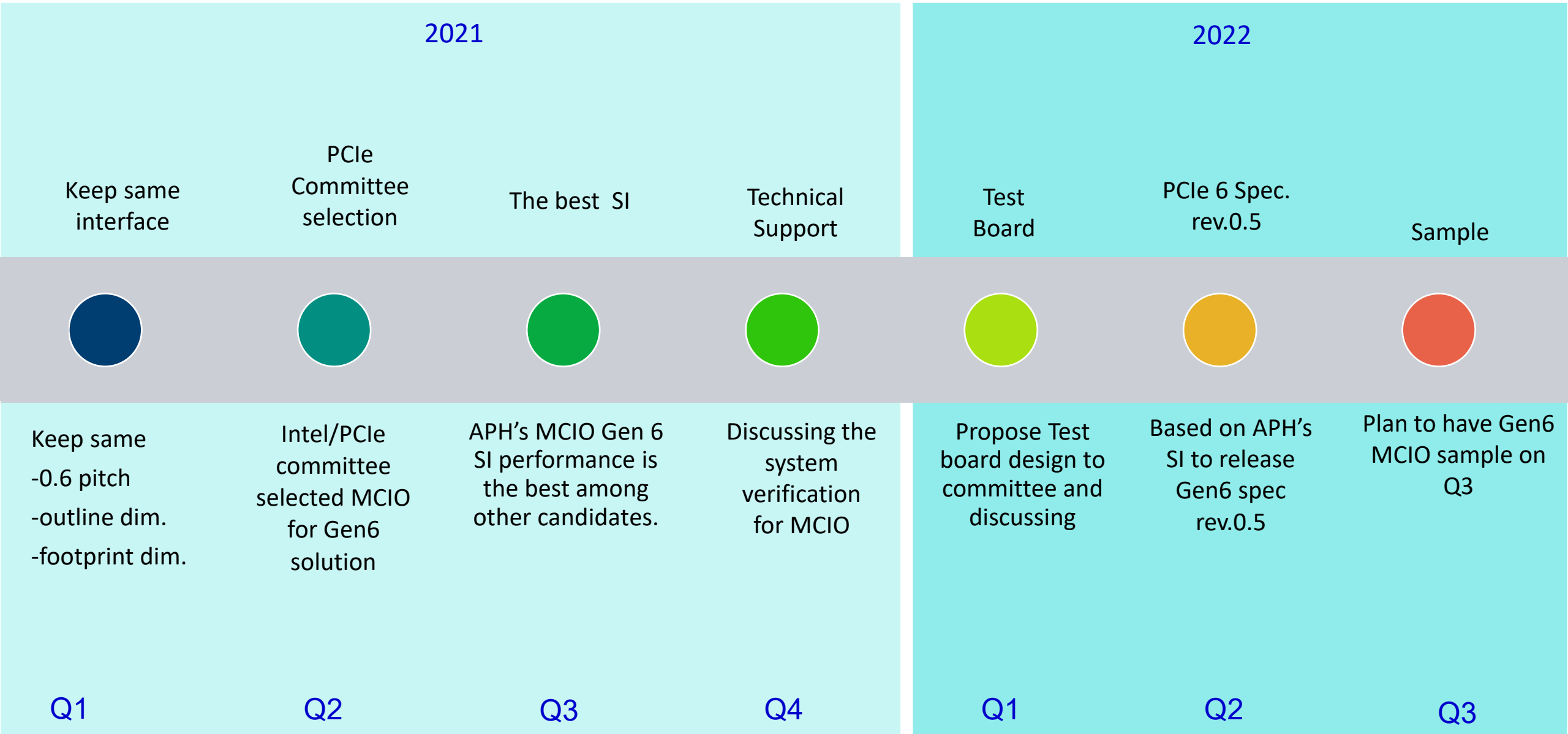
Background

- EWG internal cable spec draft Ver 0.5 proposed Gen 5 and Gen 6 MCIO cable assembly and connector SI limit
- The proposed MCIO Gen 5 cable assembly SI limits are based Rev C simulation model Amphenol provided
 - Manufacture process, material and test method variation could cause the measurement data to deviate from the simulation model
 - The Rev C model represents cable assembly with vertical receptacle connector. The spec need to cover the assembly with R/A receptacle connector as well.
- This presentation shares measurement data collected on 30 AWG cable assembly. There is gap to meet EWG Ver 0.5 draft Gen 5 proposal.
- Amphenol and some other connector vendors already deployed Gen 5 product in the field. To meet the proposal will require significant engineering development time and reinvest the tooling.
- Amphenol propose relaxed limit lines based on the measurement data



- ✓ PCIe select MCIO to be Gen6 solution.
- ✓ MCIO Gen 6 SI performance from Amphenol is the best among vendors.

Benefit and Advantage Summary

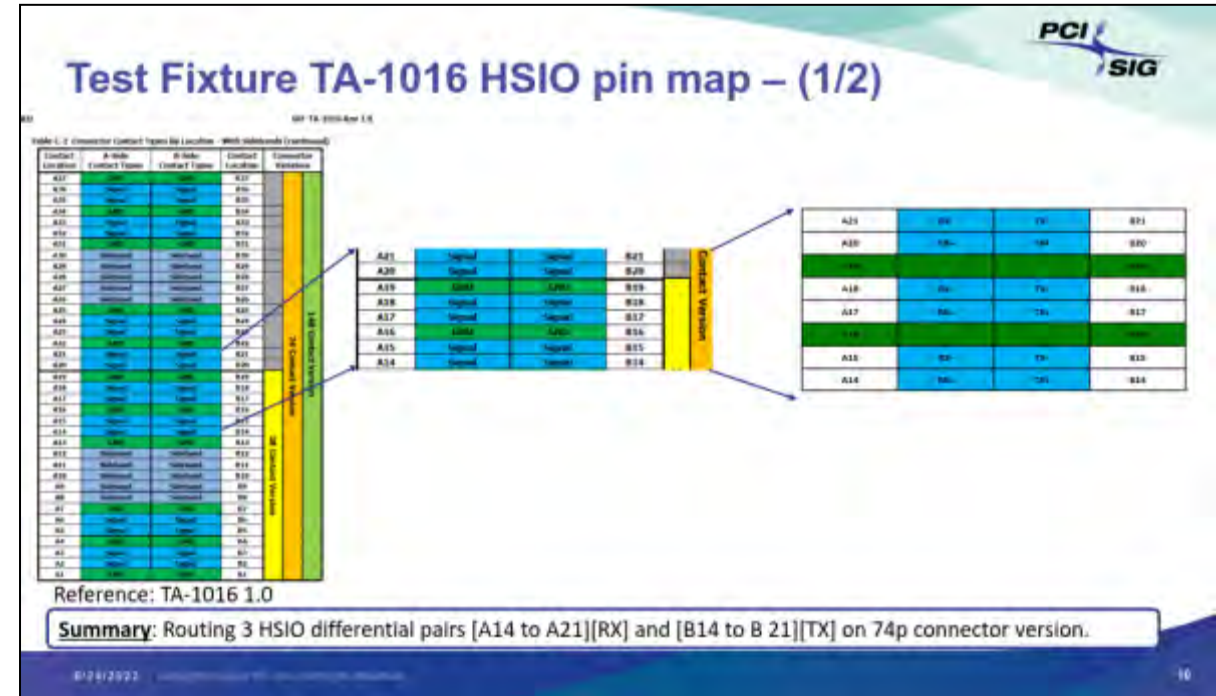


Benefit_ Co-developed with the association Test board design

- ✓ Amphenol is co-working with PCIe committee for test fixture design.

Internal Cable Test Fixture Design Matrix (1/2)

Sr. No.	Item	Item Description
1	Connector	TA-1016 connector Reference document (SFF-TA-1016 Rev 1.0)
2	Connector contact configuration	74p connector
3	Connector configuration	Vertical and Right Angle
4	Connector termination style (Vertical and Right angle)	Surface mount
5	No. of HSIO routed	3 TX and 3 RX
6	Crosstalk structure	3 NEXT and 2 FEXT
8	Voiding scheme	Reference Amphenol (slide 8)



- ✓ In the initial phase, Amphenol proposed test board design to Intel and the Committee.
- ✓ Ever since the spec of Gen 6 was defined, we have been working on a serial of tests with stricter spec
- ✓ As Amphenol has a technological breakthrough on crosstalk test, currently the Committee has adopted Amphenol’s design as a benchmark.

*Multi-Trak*TM

SFF-TA-1033/OCP-MHS

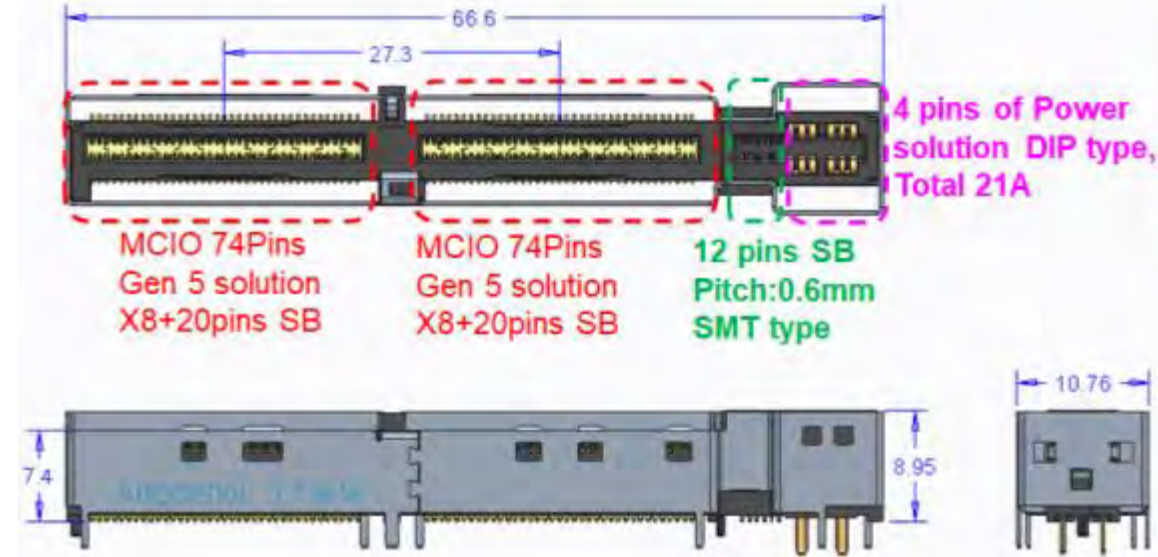
Multi-Trak™ Introduction

(SFF-TA-1033)

Amphenol CS introduces to the market the next generation interconnect solution – **Multi-Trak™**, which is a combo connector which include two of standard MCIO, 12Pins of SB and 4Pins of Power to support the combine function to reduce the limited space.

0.60 mm pitch for STD MCIO and SB, combination form factor capable of transmitting high-speed signal up to **PCIe Gen 5** and target for **PCIe Gen6**.

Total support **21A power** per current design, modularized expansion for SB and Power.



32Gbps

NRZ (Ready)

Upgrade to PCIe GEN6

64Gbps

PAM4(developing)

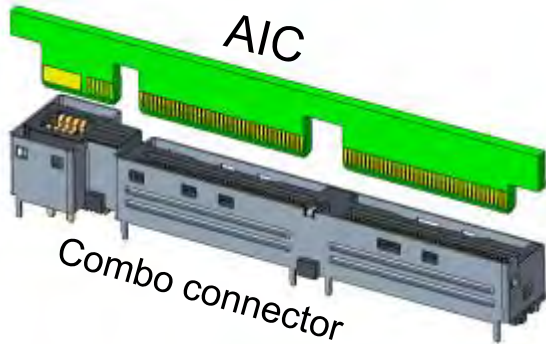
Features

- Pitch 0.60 mm, combo connector
- Up to PAM4 56Gbps, over 1 m transmission distance
- Dual-use, supporting both cable and card edge connection with one identical connector
- Target to standard form factor, covering most common uses applications in data centers such as PCIe/NVMe/OCP NIC...etc.

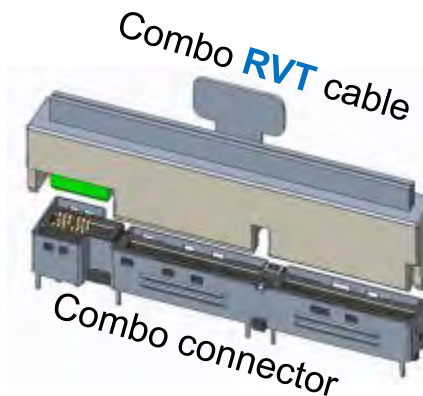
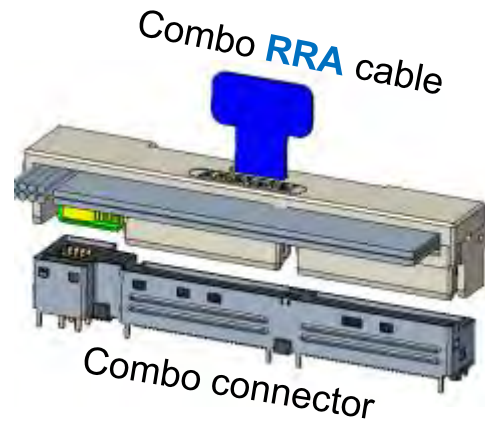
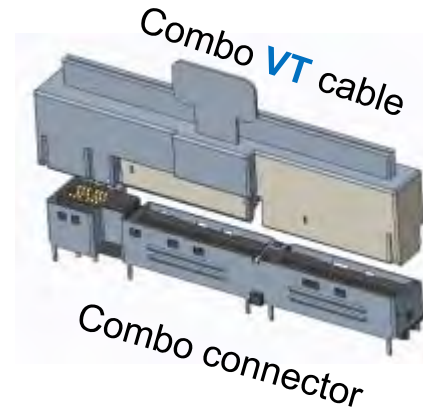
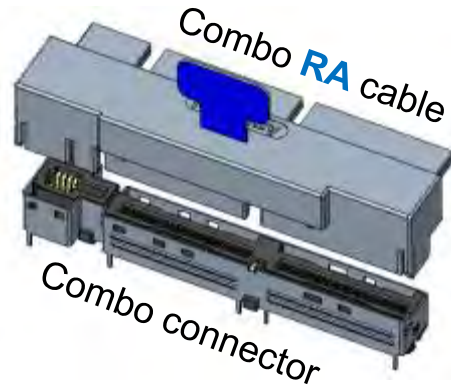
Benefits

- Providing enhanced flexibility in system design to meet highly modularized, highly scalable, and easy repairing requirement simultaneously
- Real economic choice for not only save system material cost but also show high succession of system electrical design that saves both engineering and certification expenses

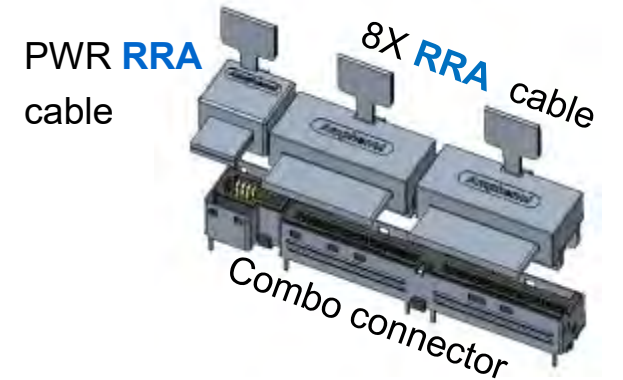
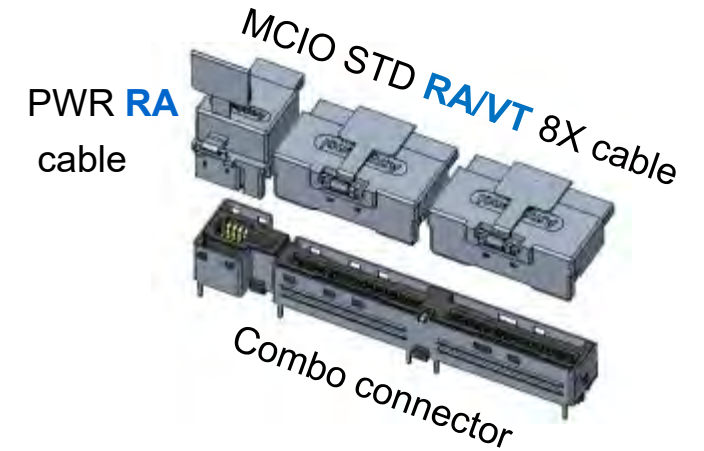
Application 1:
One AIC plug in a
combo connector

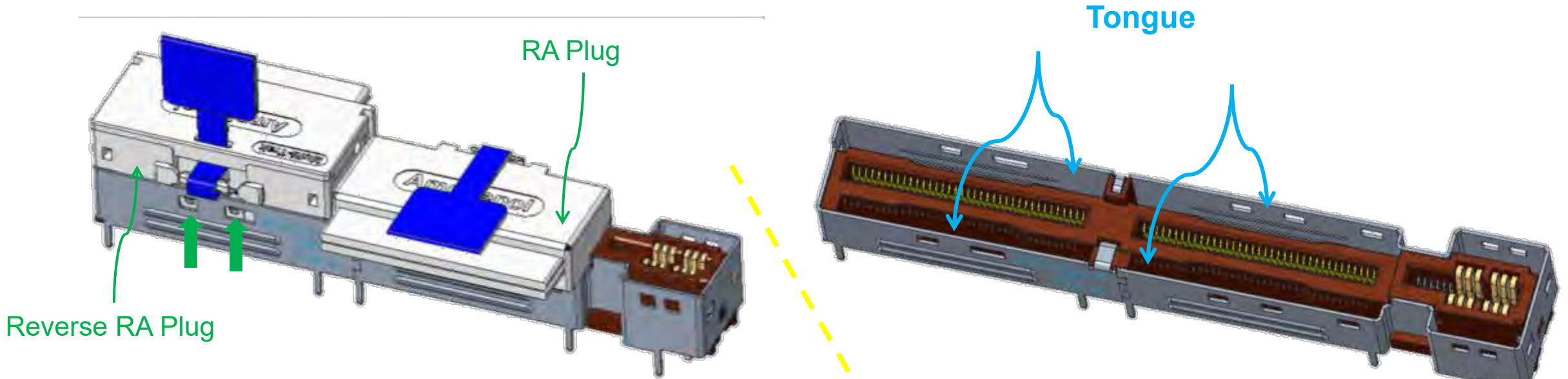


Application 2:
Combo cable

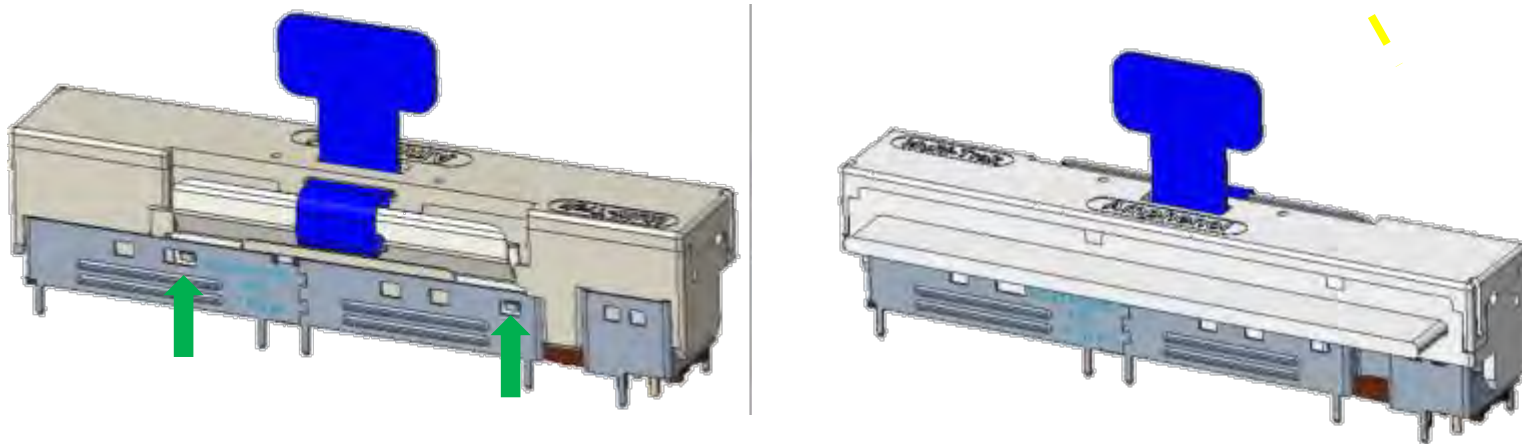


Application 3:
STD MCIO 2*8X cable





latch holes



**Fool-proof design features
for plugs mating:**

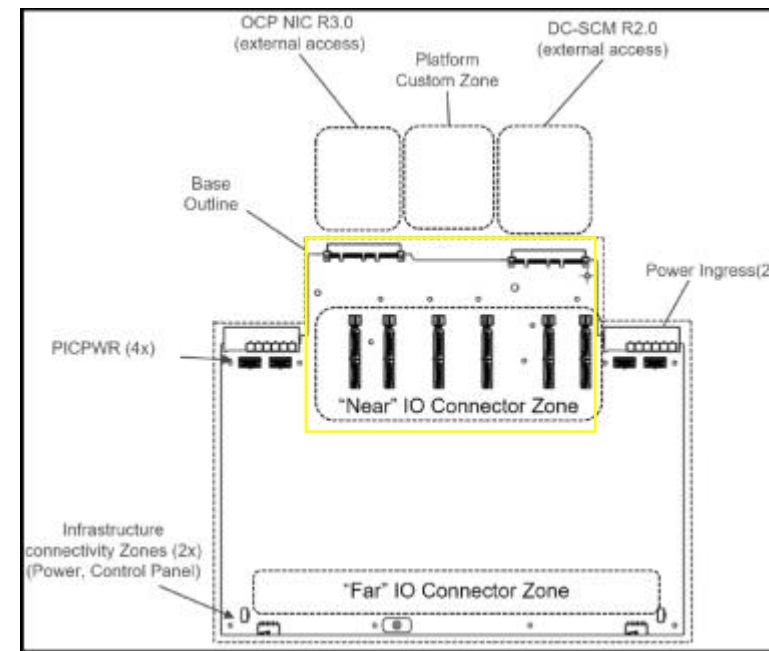
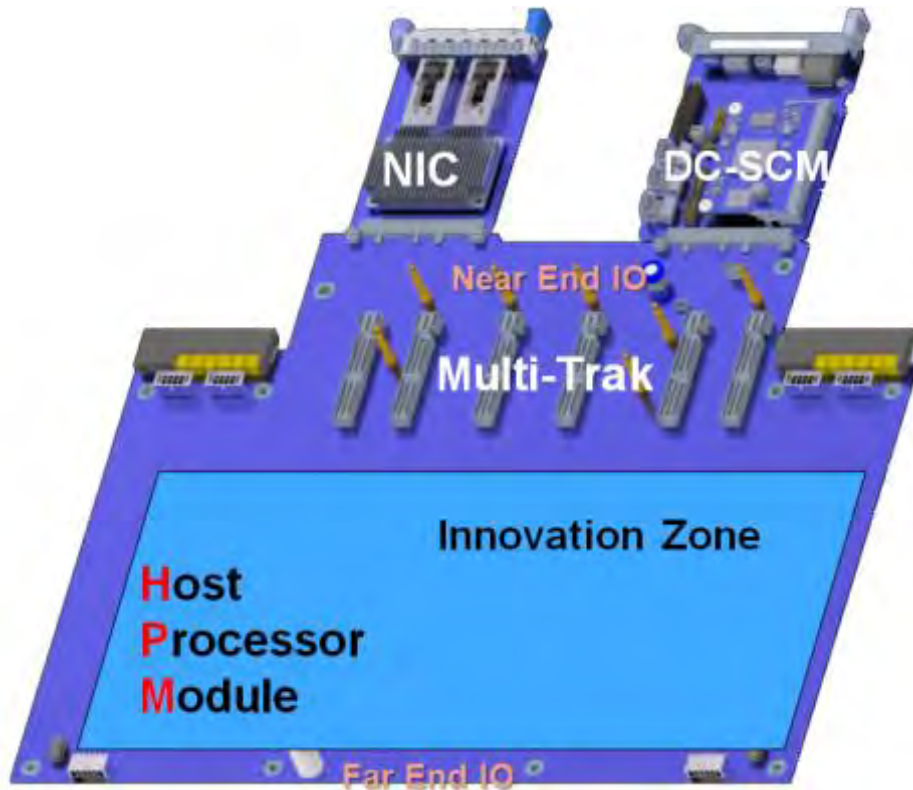
Latch holes & Tongue

Receptacle connector and two kinds of plug (RA & Reverse RA) have fool-proof design features, which can avoid two kinds of plug misuse.

Multi-Trak™ Introduction

OCP (DC-MHS)

Data Center - Modular Hardware System suggest Multi-Trak™ use to Near End side.



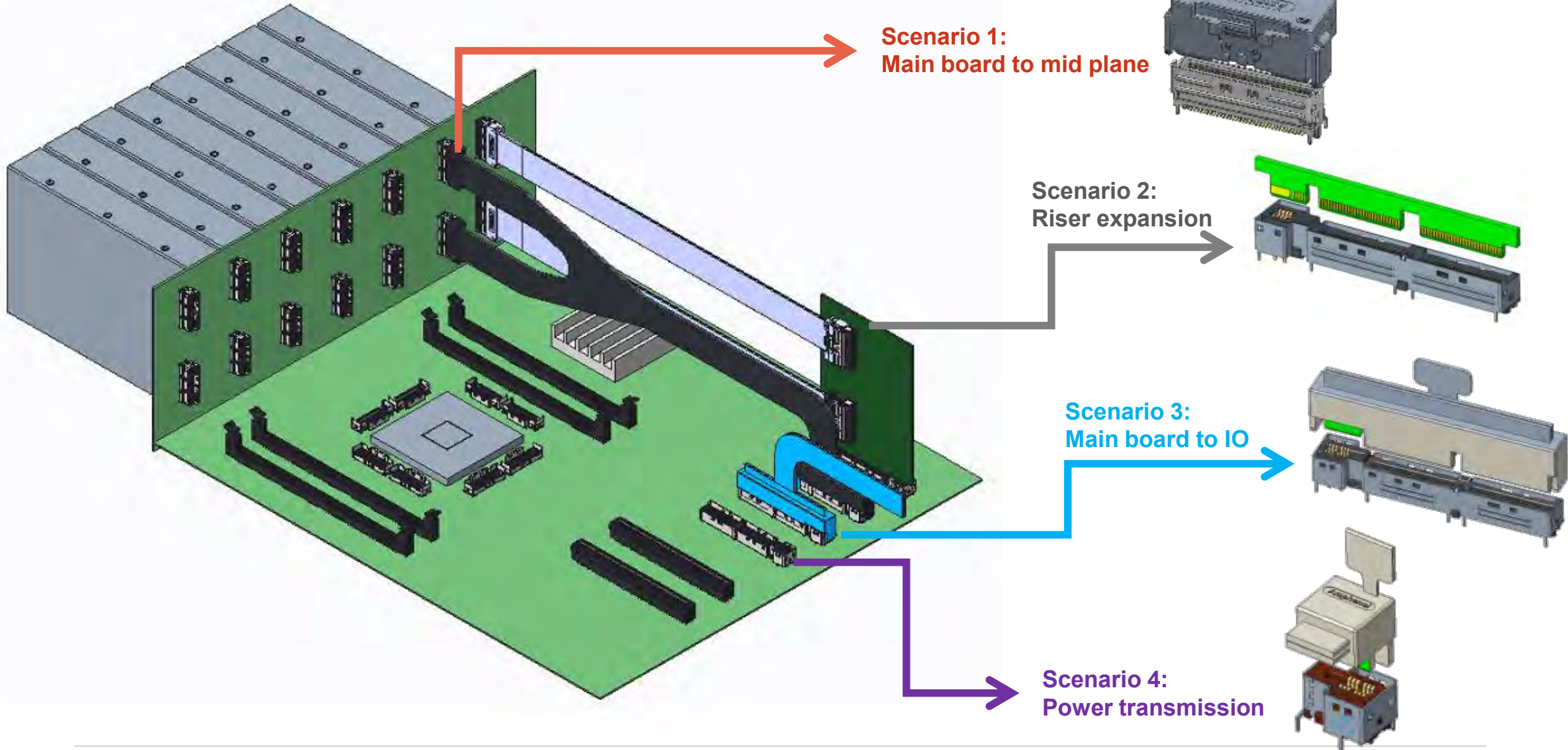
10.12.1. Location of Near Side M-XIO Connectors

Note, that Near IO Requirements are mechanically focused to enable reuse of chassis and IO subsystems.

- 1) The required connector for Near IO Riser positions shall be SFF-TA-1033.
 - a) This Near IO connector can support either rigid or cabled riser connections.
- 2) An HPM might not use all 6x Near IO positions, but designers are recommended to use maximum number of possible positions. For Near IO implemented positions, the Near IO Connector shall be placed at locations defined in Figure 18.
- 3) Additional and/or Alternate connectors used within the Near IO zone are allowed.
 - Alternate connector types, location and use cases are outside the scope of this specification.
- 4) Adoption of the following allocation priority in is recommended. Following this recommendation may result in increased applicability and interoperability of the HPM.

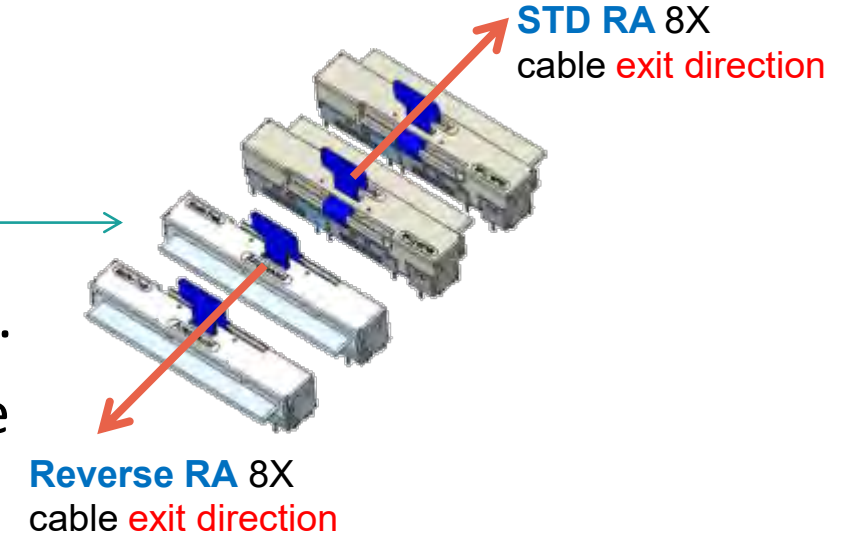
15 The Required connector for Near IO positions shall be SFF-TA-1033.

Application_Traditional Server layout reference




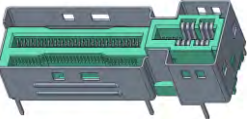
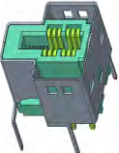
Benefit to customer

- ✓ Combine original PCIE and MCIO to be one connector, include POWER and high/low speed signal.
- ✓ Reverse cable for easy to organize the layout.
- ✓ Variety of plugs to support different routing requirement.
- ✓ Modularized design for further expansion, card and cable interactive support.
- ✓ Upgrade to **Gen6** version and apply to **PCI SIG** to be a standard connector.
- ✓ Support different applications for **AIC**, **Combo cable** and **MCIO STD cable**.
- ✓ We are discussing Multi-Trak™ with **Intel**, **WSP** and **Server** customer.

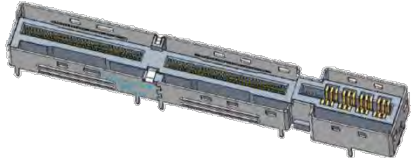




	Combo cable	STD Cable
AIC	Reverse combo cable	Reverse cable

◆ **Tooled up**

Type	Current Rating	Sample schedule
16X+Power(STD) (SFF-TA-1033) 	21A	Oct-mid
8X+Power(STD) (SFF-TA-1033) 	21A	End of Nov
Power(STD) (SFF-TA-1033) 	21A	Oct-end

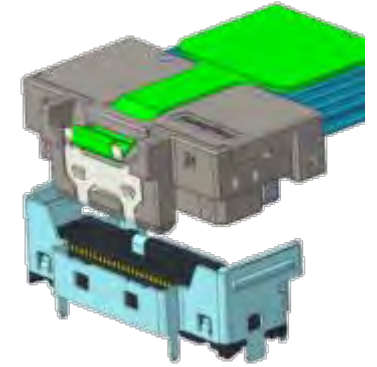
◆ **Design Ready**

Type	Status
16X+high power (Customized) 	Tool up per request
High Power (Customized) 	Tool up per request
RA type 8X+Power(STD) 	Tool up per request

ExtremePortTM Swift Series

ExtremePort™ Swift Series

Amphenol CS introduces to the market the next generation interconnect solution – **ExtremePort™ Swift**, which is 0.60 mm pitch, extreme low-profile factor yet capable of transmitting high-speed signal up to **PCIe Gen 5** and target for **PCIe Gen6** under extreme mechanical condition.



The ExtremePort™ Swift provides not only a SI performance ready signal transmission media but also a new way of system design thinking that will lead your electronic system to a completely **cost-effective, highly modularized & scalable**, and extremely **easy repairing** masterpiece.

32G_{bps}
NRZ (Ready)

64G_{bps}
PAM4 (Tooling)

112G_{bps}
PAM4 (Future development)



High Density
on one identical connection

Data Center Applications Supported:

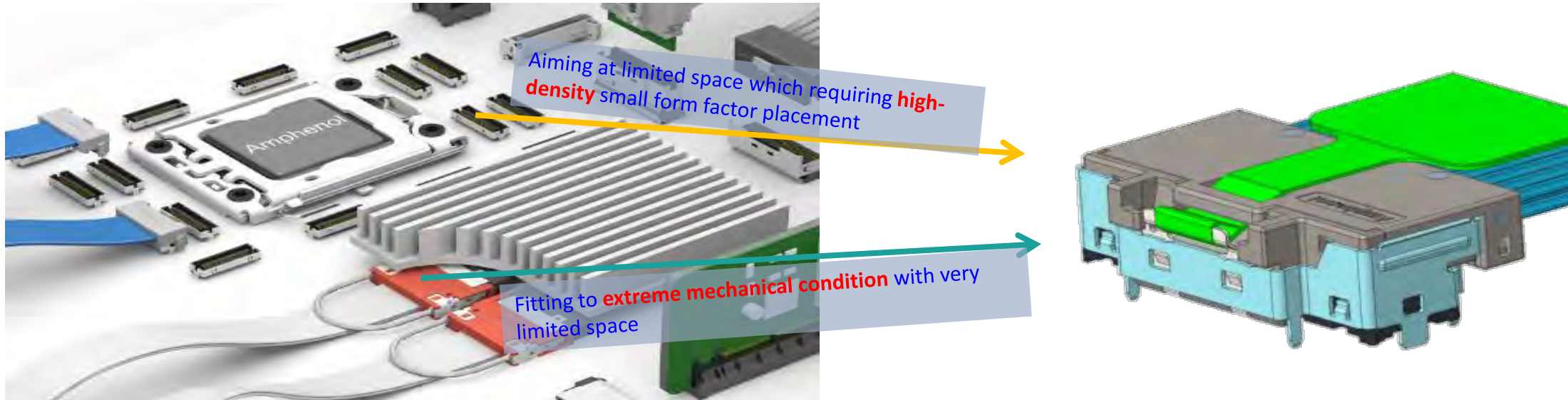
- ✓ **PCI-Express**
- ✓ **NVMe**
- ✓ **UPI**
- ✓ **Ethernet**
- ✓ **SAS**

Features

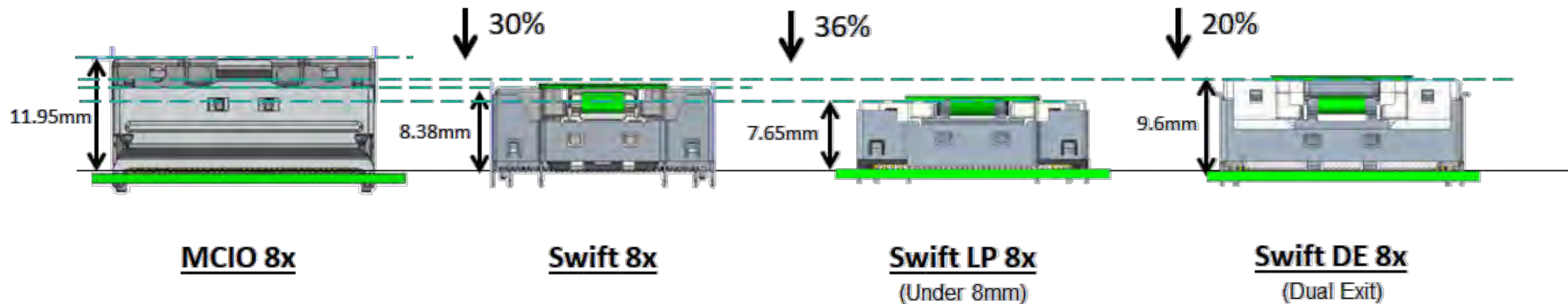
- Pitch 0.60 mm with V/T low profile form factors
- Up to NRZ 32G, over 1 m transmission distance
- Covering most common uses applications in data centers/... such as PCIe/NVMe/UPI/SAS/Ethernet/...

Benefits

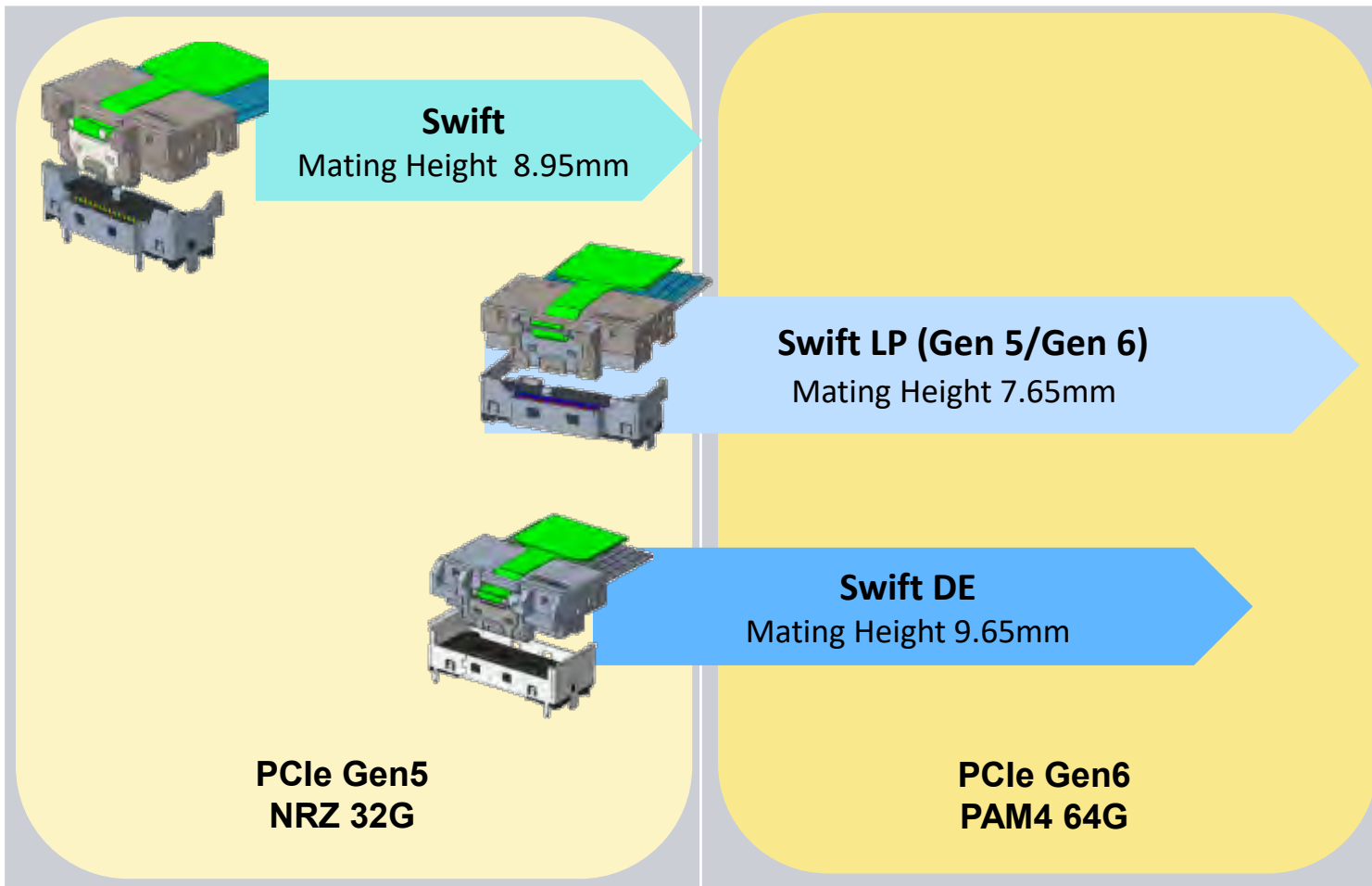
- Providing enhanced flexibility in system design to meet highly modularized, highly scalable, and easy repairing requirement simultaneously
- Real economic choice for not only save system material cost but also show high succession of system electrical design that saves both engineering and certification expenses



- Mating height comparison: MCI0(11.95mm) > Swift DE(9.6mm) > Swift(8.38mm) > Swift LP(7.65mm)

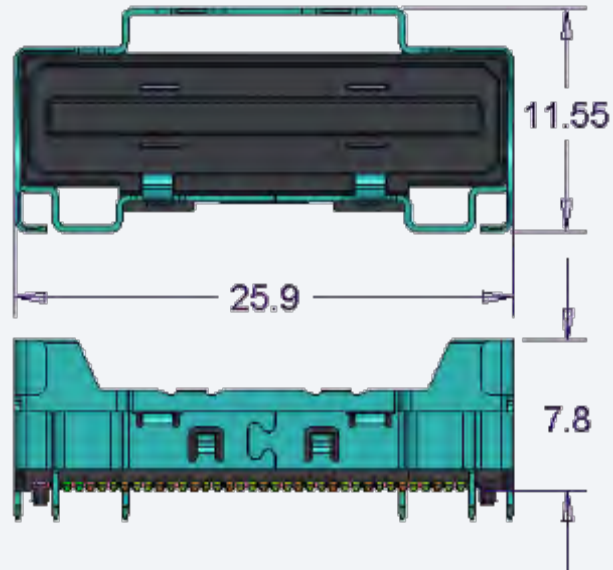


Product Supported RoadMap with PCIe Generations

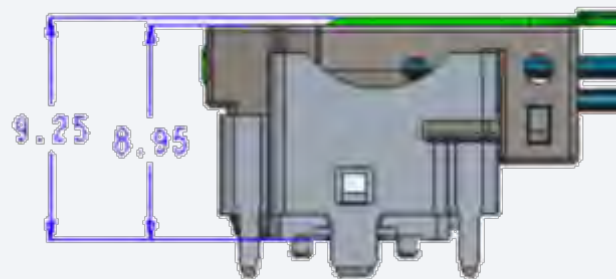


- Swift is target for near the chip and under heatsink solution with mating height mating height 8.95mm.
- Swift LP is under modifying SI for PCIe Gen 6 spec with extra low profile function (mating height 7.65 mm).
- Swift DE is our new concept for supporting customer flexible cable layout solutions

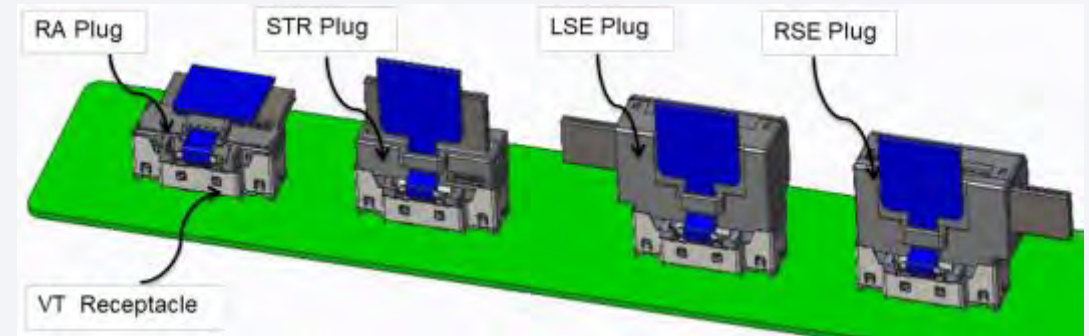
Outline Dimension:



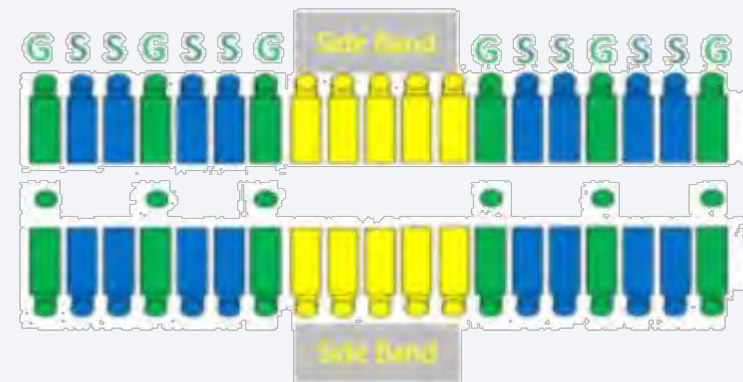
Mating Dimension:

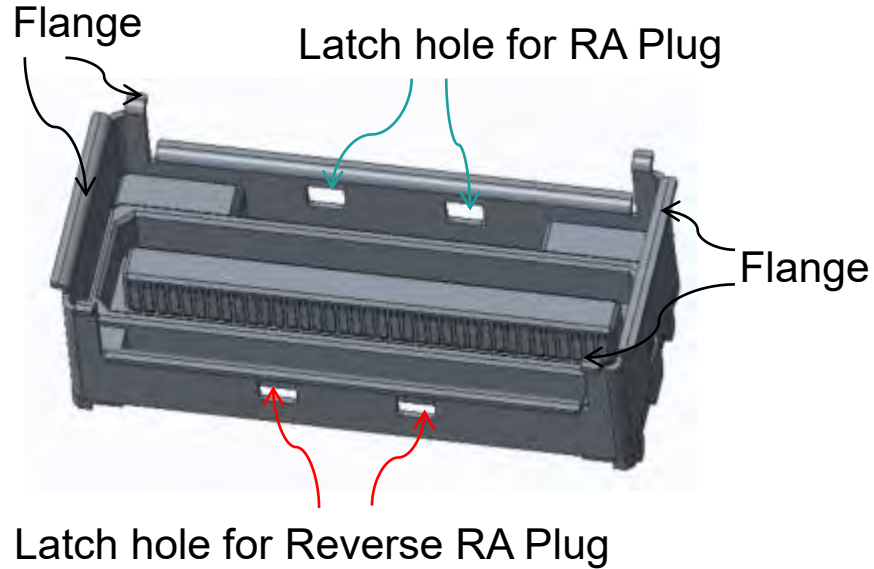


- Swift Connector only have VT parts, but have various Plug side types to support different situations

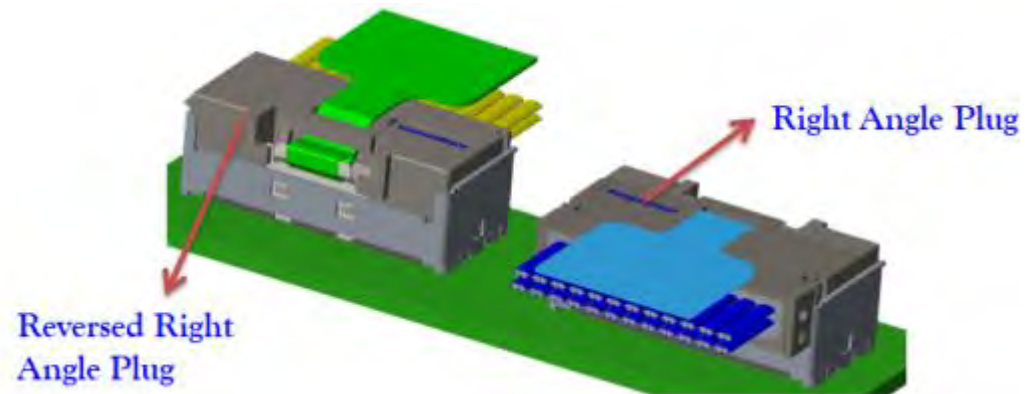
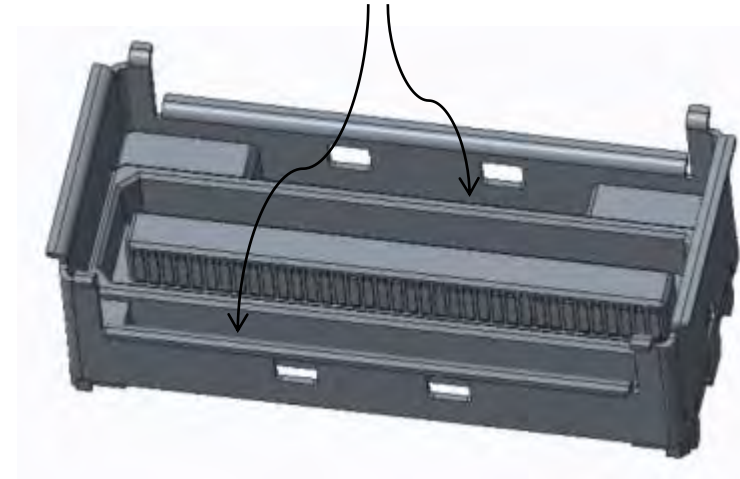


- Swift Ground Pin are connected together, but can be chosen as x4 + sideband or x6 w/o sideband (Take 38pin as example)





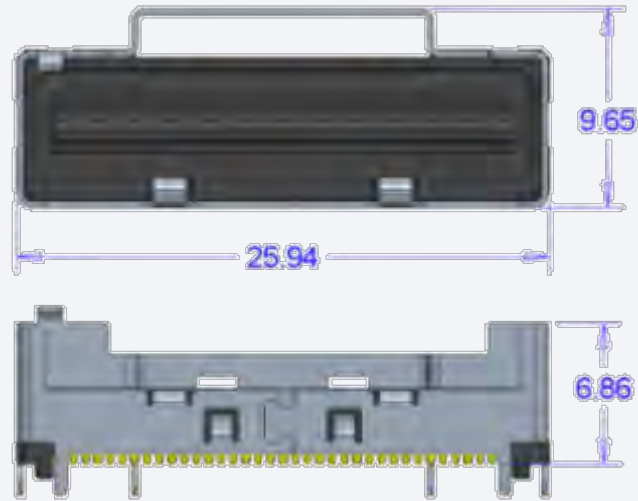
Fool-proof design features for plugs mating



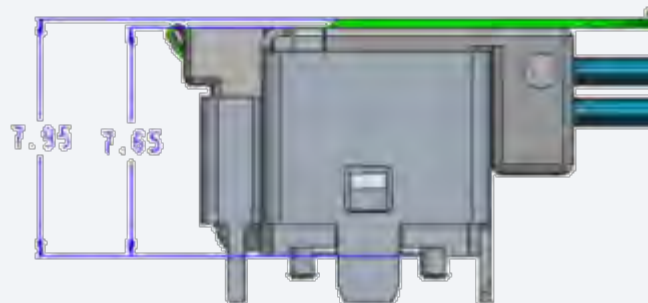
Comment:

1. Receptacle connector and two kinds of plug (RA & Reverse RA) have fool-proof design features, which can avoid two kinds of plug misuse.
2. Receptacle metal shell has a flange that it can be used for blind mating application.

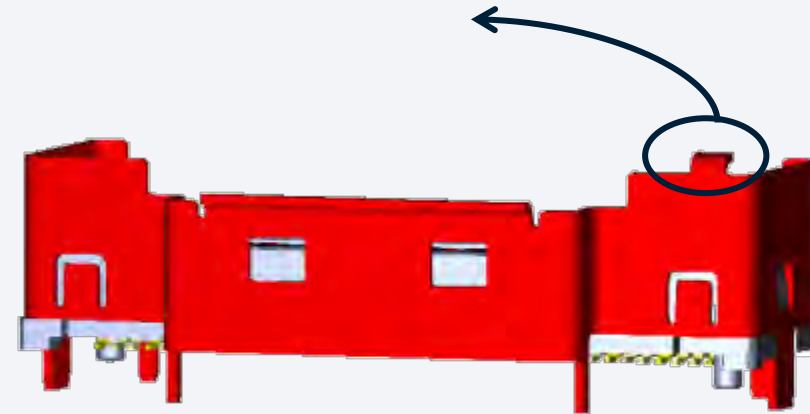
Outline Dimension:



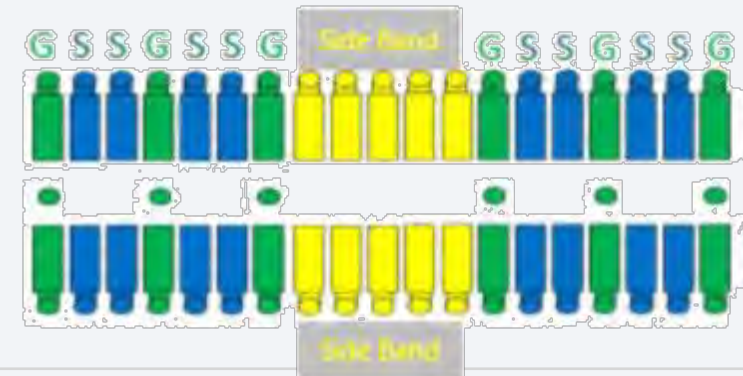
Mating Dimension:



Fool-proof design features for plugs mating



- Swift LP Ground Pin are connected together, but can be chosen as x4 + sideband or x6 w/o sideband (Take 38pin as example)



Product Roadmap

Product RoadMap		Swift (Under 9mm)			Swift DE (Flexible cable layout)			Swift LP (Under 8mm)		
		Plug		Receptacle	Plug		Receptacle	Plug		Receptacle
Type	Positions	Straight	Right Angle	Vertical	Right Angle	Reverse Right Angle	Vertical	Straight	Right Angle	Vertical
4x+Sideband or 6x w/o Sideband	38	Tool on request	Tool on request	Tool on request	Tool on request	Tool on request	Tool on request	Design Stage	Target 2022 Q4	Target 2022 Q4
8x+Sideband or 12x w/o Sideband	74	Available	Available	Available	Available	Available	Available	Design Stage	Available	Available
16x+Sideband or 20x w/o Sideband	124	Tool on request	Available	Available	Tool on request	Tool on request	Tool on request	Design Stage	Target 2022 Q4	Target 2022 Q4
20x+Sideband or 24x w/o Sideband	148	Tool on request	Tool on request	Tool on request	Tool on request	Tool on request	Tool on request	Design Stage	Target 2023 Q1	Target 2023 Q1
Wire Gauge Supported		29~34 AWG (Prefer 30~32 AWG, 34AWG is expensive due to lower yield rate and heavier labor)								
Termination Process		Support Lase Welding, Resistance Welding and Hot Bar								
Wiping Length		0.88mm								

- World No1 (30% market share in Internal HS Link)
- 1st Gen6 product released in the industry
- Co-developed with the Association and Chipset leader
- Technical Leading
- Good relationship with customers

Thank you!

For more information, please visit <https://www.amphenol-cs.com>



Commercial IO

Amphenol
COMMUNICATIONS SOLUTIONS